ROM (Read Only Memory)

- **Read-only memory** (usually known by its acronym, **ROM**) is a class of **storage** media used in **computers** and other electronic devices.
- Because data stored in ROM cannot be modified (at least not very quickly or easily), it is mainly used to distribute **firmware**.
- Firmware is **software** that is very closely tied to specific **hardware**, and unlikely to require frequent updates.
• In its strictest sense, ROM refers only to **mask ROM** (the oldest type of **solid state** ROM), which is **fabricated** with the desired data permanently stored in it, and thus can never be modified.

• However, more modern types such as **EPROM** and **flash EEPROM** can be erased and re-programmed multiple times; they are still described as "read-only memory" because the reprogramming process is generally infrequent, comparatively slow, and often does not permit **random access** writes to individual memory locations.

• Despite the simplicity of mask ROM, **economies of scale** and **field-programmability** often make reprogrammable technologies more flexible and inexpensive, so that mask ROM is rarely used in new products as of 2007.
• Classic **mask-programmed ROM** chips are integrated circuits that physically encode the data to be stored, and thus it is impossible to change their contents after fabrication. Other types of **non-volatile** solid-state memory permit some degree of modification:

Types of ROM

**Programmable read-only memory** (PROM), or **one-time programmable ROM** (OTP), can be written to or **programmed** via a special device called a **PROM programmer**. Typically, this device uses high voltages to permanently destroy or create internal links (**fuses** or **antifuses**) within the chip. Consequently, a PROM can only be programmed once.
• **Erasable programmable read-only memory** (EPROM) can be erased by exposure to strong **ultraviolet** light (typically for 10 minutes or longer), then rewritten with a process that again requires application of higher than usual voltage. Repeated exposure to UV light will eventually wear out an EPROM, but the **endurance** of most EPROM chips exceeds 1000 cycles of erasing and reprogramming. EPROM chip packages can often be identified by the prominent **quartz** "window" which allows UV light to enter. After programming, the window is typically covered with a label to prevent accidental erasure.

• **Electrically erasable programmable read-only memory** (EEPROM) is based on a similar semiconductor structure to EPROM, but allows its entire contents (or selected **banks**) to be electrically erased, then rewritten electrically, so that they need not be removed from the computer (or camera, MP3 player, etc.). Writing or **flashing** an EEPROM is much slower (milliseconds per bit) than reading from a ROM or writing to a RAM (nanoseconds in both cases).
• **Electrically alterable read-only memory** (EAROM) is a type of EEPROM that can be modified one bit at a time. Writing is a very slow process and again requires higher voltage (usually around 12 V) than is used for read access. EAROMs are intended for applications that require infrequent and only partial rewriting. EAROM may be used as non-volatile storage for critical system setup information; in many applications, EAROM has been supplanted by CMOS RAM supplied by mains power and backed-up with a lithium battery.

• **Flash memory** (or simply flash) is a modern type of EEPROM invented in 1984. Flash memory can be erased and rewritten faster than ordinary EEPROM, and newer designs feature very high endurance (exceeding 1,000,000 cycles). Modern NAND flash makes efficient use of silicon chip area, resulting in individual ICs with a capacity as high as 16 GB as of 2007[^update]; this feature, along with its endurance and physical durability, has allowed NAND flash to replace magnetic in some applications (such as USB flash drives). Flash memory is sometimes called flash ROM or flash EEPROM when used as a replacement for older ROM types, but not in applications that take advantage of its ability to be modified quickly and frequently.
DRAM

- Dynamic random access memory (DRAM) is a type of random access memory that stores each bit of data in a separate capacitor within an integrated circuit. Since real capacitors leak charge, the information eventually fades unless the capacitor charge is refreshed periodically. Because of this refresh requirement, it is a dynamic memory as opposed to SRAM and other static memory.
Types of DRAM

- Asynchronous DRAM
- Fast Page Mode (FPM) DRAM or FPRAM
- Extended Data Out (EDO) DRAM
- Burst EDO (BEDO) DRAM
- Synchronous Dynamic RAM (SDRAM)
- Direct Rambus DRAM (DRDRAM)
- Double Data Rate (DDR) SDRAM
Asynchronous DRAM

- This is the basic form, from which all others are derived. An asynchronous DRAM chip has power connections, some number of address inputs (typically 12), and a few (typically 1 or 4) bidirectional data lines. There are four **active low** control signals
**Fast Page Mode (FPM) DRAM or FPRAM**

- **Fast page mode DRAM** is also called FPM DRAM, Page mode DRAM, Fast page mode memory, or Page mode memory.

- In page mode, a row of the DRAM can be kept "open" by holding /RAS low while performing multiple reads or writes with separate pulses of /CAS. so that successive reads or writes within the row do not suffer the delay of precharge and accessing the row. This increases the performance of the system when reading or writing bursts of data.
Extended Data Out (EDO) DRAM

- **EDO DRAM** is similar to Fast Page Mode DRAM with the additional feature that a new access cycle can be started while keeping the data output of the previous cycle active. This allows a certain amount of overlap in operation (pipelining), allowing somewhat improved performance. It was 5% faster than Fast Page Mode DRAM, which it began to replace in 1993.
Burst EDO (BEDO) DRAM

• An evolution of the former, Burst EDO DRAM, could process four memory addresses in one burst, for a maximum of 5-1-1-1-1, saving an additional three clocks over optimally designed EDO memory. It was done by adding an address counter on the chip to keep track of the next address. BEDO also added a pipelined stage allowing page-access cycle to be divided into two components.
Synchronous Dynamic RAM (SDRAM)

- **SDRAM** refers to synchronous **dynamic random access memory**, a term that is used to describe dynamic random access memory that has a synchronous interface. Traditionally, dynamic random access memory (**DRAM**) has an asynchronous interface which means that it responds as quickly as possible to changes in control inputs. SDRAM has a synchronous interface, meaning that it waits for a clock signal before responding to control inputs and is therefore synchronized with the computer's system bus. The clock is used to drive an internal **finite state machine** that pipelines incoming instructions. This allows the chip to have a more complex pattern of operation than asynchronous **DRAM** which does not have a synchronized interface.
Direct Rambus DRAM (DRDRAM)

- The first PC motherboards with support for RDRAM debuted in 1999. They supported PC-800 RDRAM, which operated at 400 MHz and delivered 1600 MB/s of bandwidth over a 16-bit bus using a 184-pin RIMM form factor. Data is transferred on both the rising and falling edges of the clock signal, a technique known as double data rate. For marketing reasons the physical clock rate was multiplied by two (because of the DDR operation); therefore, the 400 MHz Rambus standard was named PC-800. This was significantly faster than the previous standard, PC-133 SDRAM, which operated at 133 MHz and delivered 1066 MB/s of bandwidth over a 64-bit bus using a 168-pin DIMM form factor.
Double Data Rate (DDR) SDRAM

- Double data rate (DDR) SDRAM was a later development of SDRAM, used in PC memory beginning in 2000. DDR2 SDRAM was originally seen as a minor enhancement (based upon the industry standard single-core CPU) on DDR SDRAM that mainly afforded higher clock rates and somewhat deeper pipelining. However, with the introduction and rapid acceptance of the multi-core CPU in 2006, it is generally expected in the industry that DDR2 will revolutionize the existing physical DDR-SDRAM standard. Further, with the development and introduction of DDR3 SDRAM in 2007, it is anticipated DDR3 will rapidly replace the more limited DDR and newer DDR2.
Like all SDRAM implementations, DDR2 stores memory in memory cells that are activated with the use of a clock signal to synchronize their operation with an external data bus. Like DDR before it, DDR2 cells transfer data both on the rising and falling edge of the clock (a technique called "double pumping"). The key difference between DDR and DDR2 is that in DDR2 the bus is clocked at twice the rate of the memory cells, so four bits of data can be transferred per memory cell cycle. Thus, without changing the memory cells themselves, DDR2 can effectively operate at twice the data rate of DDR
<table>
<thead>
<tr>
<th>Standard name</th>
<th>Memory clock</th>
<th>Cycle time</th>
<th>I/O Bus clock</th>
<th>Data transfers per second</th>
<th>Module name</th>
<th>Peak transfer rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR2-400</td>
<td>100 MHz</td>
<td>10 ns</td>
<td>200 MHz</td>
<td>400 Million</td>
<td>PC2-3200</td>
<td>3200 MB/s</td>
</tr>
<tr>
<td>DDR2-533</td>
<td>133 MHz</td>
<td>7.5 ns</td>
<td>266 MHz</td>
<td>533 Million</td>
<td>PC2-4200, PC2-4300¹</td>
<td>4266 MB/s</td>
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<tr>
<td>DDR2-667</td>
<td>166 MHz</td>
<td>6 ns</td>
<td>333 MHz</td>
<td>667 Million</td>
<td>PC2-5300, PC2-5400¹</td>
<td>5333 MB/s</td>
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<tr>
<td>DDR2-800</td>
<td>200 MHz</td>
<td>5 ns</td>
<td>400 MHz</td>
<td>800 Million</td>
<td>PC2-6400</td>
<td>6400 MB/s</td>
</tr>
<tr>
<td>DDR2-1066</td>
<td>266 MHz</td>
<td>3.75 ns</td>
<td>533 MHz</td>
<td>1066 Million</td>
<td>PC2-8500, PC2-8600¹</td>
<td>8533 MB/s</td>
</tr>
</tbody>
</table>
• DDR3 memory provides a reduction in power consumption of 30% compared to DDR2 modules due to DDR3's 1.5 V supply voltage, compared to DDR2's 1.8 V or DDR's 2.5 V. The 1.5 V supply voltage works well with the 90 nanometer fabrication technology used in the original DDR3 chips. Some manufacturers further propose using "dual-gate" transistors to reduce leakage of current.

• DDR3 modules can transfer data at a rate of 800–1600 MHz using both rising and falling edges of a 400–800 MHz I/O clock. In comparison, DDR2's current range of data transfer rates is 400–800 MHz using a 200–400 MHz I/O clock, and DDR's range is 200–400 MHz based on a 100–200 MHz I/O clock.
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<tbody>
<tr>
<td>DDR3-800</td>
<td>100 MHz</td>
<td>10 ns</td>
<td>400 MHz</td>
<td>800 Million</td>
<td>PC3-6400</td>
<td>6400 MB/s</td>
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<tr>
<td>DDR3-1066</td>
<td>133 MHz</td>
<td>7.5 ns</td>
<td>533 MHz</td>
<td>1066 Million</td>
<td>PC3-8500</td>
<td>8533 MB/s</td>
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<tr>
<td>DDR3-1333</td>
<td>166 MHz</td>
<td>6 ns</td>
<td>667 MHz</td>
<td>1333 Million</td>
<td>PC3-10600</td>
<td>10667 MB/s[1]</td>
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<tr>
<td>DDR3-1600</td>
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<td>5 ns</td>
<td>800 MHz</td>
<td>1600 Million</td>
<td>PC3-12800</td>
<td>12800 MB/s</td>
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